C. Amendments to the Claims.

49. (**Currently Amended**) A method for making a non-volatile semiconductor device comprising:

forming a multilayer gate dielectric having a charge storage layer and being dielectrically equivalent to a layer of silicon dioxide having a thickness that is less than 200 angstroms;

forming a gate comprising polycrystalline silicon of **a** first conductivity type on said gate dielectric; and

forming source and drain regions separated by a channel region in a semiconductor substrate, said source and drain regions having a second conductivity type different from said first conductivity type.

50. (Original) The method of claim 49, wherein:

forming the multilayer gate dielectric includes forming a bottom dielectric, the charge storage layer over the bottom dielectric, and a top dielectric over the charge storage layer.

51. (Original) The method of claim 50, wherein:

forming the bottom dielectric includes forming a layer of silicon dioxide.

52. (Original) The method of claim 50, wherein:

forming the bottom dielectric includes thermally growing a layer of silicon dioxide.

53. (Original) The method of claim 50, wherein:

forming the charge storage layer includes forming a

layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.

54. (Original) The method of claim 50, wherein:

forming the top dielectric includes forming a layer of silicon dioxide.

55. (**Currently Amended**) The method of claim 54, wherein:

forming the top dielectric includes thermally growing **[a]** **the** layer of silicon dioxide.

56. (**Currently Amended**) The method of claim 54, wherein:

forming the top dielectric includes depositing **[a]** **the** layer of silicon dioxide.

57. (Original) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate doped to an n-type conductivity; and

the source and drain regions have a p-type conductivity.

58. (Original) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate doped to a p-type conductivity; and

the source and drain regions have an n-type conductivity.

59. (Original) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate having a dopant concentration greater than about 10^{10} atoms/cm^3.

60. (**Withdrawn**) A method, comprising the steps of:

applying an electric field to a charge storage layer in a multilayer dielectric disposed between a first semiconductor layer and a second semiconductor layer to form a charge accumulation region in the first semiconductor layer proximate to the multilayer gate dielectric and a charge depletion region in the second semiconductor layer proximate to the multilayer gate dielectric.

61. (**Withdrawn**) The method of claim 60, wherein:

the first semiconductor layer comprises a transistor gate; and

the second semiconductor layer comprises a transistor channel between a source and drain region.

62. (**Withdrawn**) The method of claim 60, wherein:

the first semiconductor layer comprises a transistor channel between a source and drain region; and

the second semiconductor layer comprises a transistor gate.

63. (**Withdrawn**) The method of claim 60, wherein:

the first semiconductor layer and second semiconductor layer are doped to a first conductivity type.

64. (**Withdrawn**) The method of claim 60, wherein:

the applying step is conducted for a length of time sufficient to accumulate charge in a charge storage layer of the multilayer dielectric.

65. (**Withdrawn**) The method of claim 64, wherein:

the applying step is conducted under conditions sufficient to tunnel electrons through a tunnel dielectric of the multilayer dielectric to the charge storage layer.

66. (**Withdrawn**) The method of claim 64, wherein:

the charge storage layer comprises silicon nitride.

67. (**Withdrawn**) The method of claim 60, wherein:

the first semiconductor layer comprises a p-type gate; and

the second semiconductor layer comprises a p-type channel disposed between n-type source/drain regions.

68. (**Withdrawn**) The method of claim 60, wherein:

the first semiconductor layer comprises an n-type gate; and

the second semiconductor layer comprises an n-type channel disposed between p-type source/drain regions.

69. (**Withdrawn**) The method of claim 60, wherein:

the multilayer gate dielectric comprises a charge storage layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.